REMARKS

Claims 19-44 are pending.

Claims 19-44 stand rejected.

Claims 19 and 28 have been amended.

No new matter has been added.

Claims 19-44 are hereby submitted for reconsideration.

In paragraph 3 of the Office Action, the Examiner has continued the rejection of claims 41 and 42 under 35 U.S.C. § 112 for failing to comply with the written description requirement. Applicants disagree with the Examiner's contention and note that the element of a plurality of modules including an interface unit, which is capable of controlling a first host processor" is supported in the specification as originally filed.

In order to address this, Applicants refer to page and column numbers from U.S. Patent No. 6,347,344, the parent patent of this application, as it contains an identical specification and for the convenience of reciting readily identifiable columns and line numbers.

For example, column 12, line 62 through column 13, line 12 of the '344 patent recites:

> "Thus, a multimedia system employing multimedia processor 100 is illustrated in FIG. 1(c), which operates with a host processor 230, such as an X86.RTM., in accordance with one embodiment of the present invention. Multimedia processor 100 is coupled to a host processor 230 via an accelerated graphics bus AGP. Processor 230 is coupled to an ISA bus via a PCI bus 260 and a south bridge unit 232. An audio I/O controller such as 218 (FIG. 1(b)) is configured to receive from and send signals to ISA bus 258 via ISA SB/Comm mapper 232 and multiplexer 136. Furthermore, I.sup.2 C/DDC driver unit 216 is configured to receive corresponding standard compliant signals via multiplexer 136. Driver unit 216 receives display data channel signals which are intended to provide signals for controlling CRT resolutions, screen sizes and aspect ratios. ISDN/GCI driver unit 221 of multimedia processor 100 is configured to receive from and send signals to an ISDN U or S/T interface unit 236"

This description is directed to the operation of the module included in an interface unit, such as a driver unit or the like, as stated in the above quoted section. Here, the specification is describing that the processing is performed by calculations using the host processor 230. Given this description, it can be reasonably considered by one of ordinary skill in the art that the interface unit of the driver unit or the like can have the host processor 230 as a slave.

Thus, for example, in the process described, the host processor 230 performs the process to have the audio I/O controller, I^2 C/DDC driver unit 216, and ISDN/GCI driver unit 221 perform calculations. The audio I/O controller I^2 C/DDC driver unit 216 and ISDN/GCI driver unit 221 are modules included in the interface unit. Such a written description should be considered to disclose that the interface unit includes modules which render the host processor as the slave. More detailed description of this process is further found on column 9, line 25 through column 13, line 12 under the heading "INTERFACE UNIT & MULTIPLEXER."

Turning to the prior art rejection, the present invention has been described in detail in previous Amendments. In addition to the previous descriptions, the present invention as claimed in independent claims 19 and 28 are further directed to a data transfer switch disposed within the multimedia processor and coupled to the second processor for transferring data to various modules of the multimedia processor, at least one of which is a data cache, where the data transfer switch is configured to transfer data between the modules of the multimedia processor in either direction between the data cache and the other module within the multimedia processor as requested by the modules.

Such an arrangement provides for the ability to make data transfer possible directly between the data cache and other modules in the processor. Thus, the subject of the transfer in the present invention ***will always include a transfer from/to a data cache to one of the other modules***.

The cited prior art namely Gibson teaches a data transfer mode for simply transferring the data utilizing a route pixel organizer 246, under the description concerning memory copy command. Thus, in order to read Gibson in such a way to have the data cache as shown in Fig. 2 to transfer data in mutual directions with the outer interface controller 238 or the local memory controller 236, the mode of transfer must be via the operand organizer B or operand organizer C.

However, according to the description for the memory copy command in Gibson, the transfer of data without processing the data is clearly described as performed by following a route ***other than t***he route of the operand organizer B or the operand organizer C. As such, Gibson teaches that the direct transfer of data itself without process of the data ***cannot be attained by the route of the operand organizer B or the operand organizer C. Thus, transferred data by the "data transfer switch" in Gibson occurs between modules NOT ALWAYS including a data cache, such as data cache 230, but instead between two non-data cache modules.***

Such teachings as disclosed in Gibson can not read on the data transfer switch of the present invention which directly transfers data between the data cache and another module of the multimedia processor.

It is noted that Kusters teaches a multiplexer unit but does not disclose material related to the data transfer switch of the present invention.

As such, even if the references were combined as suggested by the Examiner the resulting structure would still not teach or suggest all of the elements of the present invention as claimed. For example, even if combined, the cited references still does not teach or suggest a data transfer switch that transfers data between two modules of the multimedia processor where at least one module is a data cache.

Applicants specifically note that they are not attempting to address the references separately as suggested by the Examiner in the Office Action. Rather Applicants are

stating that the references, as combined by the Examiner, do not teach or suggest all of the elements of the claim. Although the comments above are directed primarily towards Gibson, that is only because the Examiner relied on Gibson to form the portion of the rejection related to the data transfer switch.

As a separate argument the present invention includes a multiplexer coupled to said interface unit for providing access between a selected number of said I/O device driver units to external I/O devices via output pins, where the I/O device driver units are provided to the interface unit directly connected to the multiplexer. Here the device driver, being the subject of the data transfer from the multiplexer, is provided to the interface unit connected to the multiplexer. The multiplexer is thus coupled to the interface unit.

Kusters on the other hand teaches that the device drivers exclude the unit coupled to the multiplexer. In Kusters the system memory and the like are located between the multiplexer and the such interfaces.

Applicants note that the Examiner himself has indicated that Gibson does not teach a multiplexer according to the present invention.

Again, even if Gibson and Kusters were combined as suggested by the Examiner, the combined reference still do not teach suggest all of the elements of the present invention as claimed. For example, even if combined, the cited references still does not teach or suggest a multiplexer coupled to said interface unit for providing access between a selected number of said I/O device driver units to external I/O devices via output pins, ***where the I/O device driver units are provided to the interface unit directly connected to the multiplexer.***

Also, Applicants again note that they are not attempting to address the references separately as suggested by the Examiner in the Office Action. Rather Applicants are stating that the references, as combined by the Examiner, do not teach or suggest all of

the elements of the claim. Although the comments above are directed primarily towards Kusters, that is only because the Examiner relied on Kusters to form the portion of the rejection related to the multiplexer.

As such, for at least these two reasons, Applicants respectfully request that the rejections to independent claims 19 and 28 be withdrawn and the rejection to the claims that depend therefrom be withdrawn as well for the same reasons.

In view of the forgoing, Applicants respectfully submit that the present invention as claimed is now in condition for allowance, the earliest possible notice of which is earnestly solicited. If the Examiner feels that a telephone interview would advance the prosecution of this application he is invited to contact the undersigned at the number listed below.

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By:

Respectfully submitted
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